WHAT IS CLAIMED IS:

1. A circuit configuration for testing a semiconductor memory, comprising:

an output register for receiving digital data;

a plurality of shift registers for serially outputting the digital data to be received by the output register, wherein each one of the plurality of shift registers includes a feedback path for enabling the digital data output by a corresponding one of the plurality of shift registers to be input back into the corresponding shift register in a same sequence as the digital data is output from the corresponding shift register.

2. The circuit configuration of claim 1, wherein each one of the plurality of shift registers has a different bit storage capacity.

3. The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 48-bit register.

4. The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 33-bit register.

5. The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 20-bit register.

6. The circuit configuration of claim 1, wherein the output register has a bit storage capacity equal to a bit storage capacity of a largest one of the plurality of shift registers.

7. The circuit configuration of claim 1, further comprising an output pin which is strobed to examine contents of the output register.

8. The circuit configuration of claim 1, further comprising a multiplexer interposed between the output register and the plurality of shift registers.

9. The circuit configuration of claim 1, wherein the semiconductor memory is a built-in self repair (BISR) memory.

10. The circuit configuration of claim 1, wherein the digital data received by the output register is divided into patterns corresponding to the plurality of shift registers.

11. A method for testing a semiconductor memory, comprising steps of:

serially outputting digital data from a shift register into an output register;

inputting the digital data back into the shift register in a same sequence as the digital data is output from the shift register; and

examining the digital data in the output register.

12. The method of claim 11, wherein the shift register is disabled while the digital data in the output register is examined.

13. The method of claim 11, wherein the semiconductor memory is a built-in self repair (BISR) memory.